IN THE SPECIFICATION:

Please amend the paragraph beginning at page 4, line 10, as follows.

FIGS. 5B and ~~6C~~ 5C illustrate circuit diagrams that exemplify the circuit of FIG. 5A in dual-port and single-port, respectively, configurations;

Please amend the paragraph beginning at page 7, line 4, as follows.

In the example of FIG. 1, there are four signal lines to each memory cell: ~~(1)~~ the write bitline, BLw; the read bitline BLr; the write control line, WLw; and the read control line, WLr. This memory cell 100 is a dual-port RAM circuit, which allows one cell to be read from while another cell (not shown) is written into. In this case, one set of cells are addressed and controlled by a wordline WLr for read operation, and another set of cells are addressed and controlled by another wordline WLw for write operation.The bitlines BLw and BLr can be combined, if desired, into one bitline, BL. The BL can serve as the combined input and output line to the memory cell 100, forming a single-port memory cell. The read bitline BLr has a capacitance of "Cbl" and a charge of "Qbl."

Please amend the paragraph beginning at page 11, line 22, as follows.

A specific predetermined voltage is applied to the read control line WLr during a write operation. The initial predetermined voltage on the read control line WLr is low (e.g., some negative voltage), and is raised to high (e.g., 0 V) during the write operation. An alternative voltage scheme is to raise the read control line from 0 V to a certain positive voltage. The key, when the write switch 110 is an NFET transistor, is a voltage increase during a write operation. Firstly, the raising of the read control line WLr from a lower voltage (e.g., the negative predetermined voltage) to a higher voltage (e.g., ground) is key to the boosting of the data one voltage, as well as turning-off the write switch 110. Secondly, such raising of the read control line WLr voltage does not boost the data zero voltage as the write switch 110 is not turned off, hence keeping the storage cell voltage at the low voltage of the bitline predetermined voltage (for ~~date~~ data zero). So if the predetermined bitline high voltage is denoted by VBLH, and low voltage is 0 V, the bitline voltage difference between data zero and data one is VBLH. For writing data one, if the boosting voltage jump on the read control line is VB, a voltage of VBLH + VB will be written to the storage cell at the end of the write operation. For writing data zero, since the boosting is only one-way, and the cell storage voltage Vcell 145 stays around 0 V. As a result, the voltage difference, corresponding to data one and data zero, stored in the storage cell is VBLH + VB, resulting a gain of (VBLH + VB)/VBLH = 1 + VB/VBLH, which is strictly larger than 1. Typically the gain is close to 2, taking into account stray capacitance around the memory circuit, as VB is about the same as VBLH. It is desirable that a smaller voltage differential on the bitline BLw between data one and data zero is amplified and stored in the storage cell as a larger voltage differential, by means of the "one-way" boosting of the read control line WLr, regardless of the write control voltage.

Please amend the paragraph beginning at page 17, line 24, as follows.

The table shown in FIG. 6 illustrates various exemplary configurations of transistors from FIGS. 3A, 3B, 4A, and 4B, with different voltages and technologies. In the table, VWLw is the voltage placed on the write control line (WLw), VTw is the threshold voltage of the write transistor, VWLr is the voltage placed on the read control line (WLr), VTr is the threshold voltage of the read transistor, ~~Vscre~~ Vsrc is the source voltage of the read transistor, Vcell is the voltage stored at location 145 of FIG. 1, VBLH is the bitline precharged voltage, VBL is the bitline voltage, and Vg_leak_read is a measure, at the gate of the read transistor, of its source-to-drain leakage current. Vg_leak_write, discussed below, is a measure, at the gate voltage of the write transistor, of its source-to-drain leakage current.